WHAT IS CLAIMED IS:

1. A processor capable of executing conditional instructions, which executes an instruction set including M-bit instructions and N-bit instructions (where M, N are positive integers, M>N), the instruction set having condition execution instructions and M-bit parallel condition execution instructions, the parallel condition execution instruction having a first N-bit instruction and a second N-bit instruction, the processor comprising:

a flag having a state;

an instruction fetching device, to fetch at least one instruction to be performed;

an instruction decoder, to decode the instruction fetched by the instruction fetching device;

an instruction executing device, to execute the instruction outputted by the instruction decoder, wherein the state of the flag is set according to a result of executing a condition execution instruction, which indicates a state of condition acceptance or rejection; and

a mode switching device, to switch the instruction decoder to decode one of the first and the second N-bit instructions according to the state of the flag, so as to be subsequently performed by the instruction executing device, when a parallel condition execution instruction is fetched by the instruction fetching device.

2. The processor as claimed in claim 1, wherein, when the instruction executing device executes a condition execution instruction, the flag is set

to a first logic state if the execution results in a condition acceptance, and set to a second logic state if the execution results in a condition rejection.

3. The processor as claimed in claim 2, wherein the first logic state is "true" and the second logic state is "false".

4. The processor as claimed in claim 2, wherein the first logic state is "false" and the second logic state is "true".

5. The processor as claimed in claim 2, wherein, when the instruction is a parallel condition execution instruction and the flag is on the first logic, the mode switching device switches the instruction decoder to decode the first N-bit instruction, so as to be subsequently performed by the instruction executing device.

6. The processor as claimed in claim 2, wherein, when the instruction is a parallel condition execution instruction and the flag is on the second logic, the mode switching device switches the instruction decoder to decode the second N-bit instruction, so as to be subsequently performed by the instruction executing device.

7. The processor as claimed in claim 2, wherein the condition execution instruction is an M-bit instruction.

8. The processor as claimed in claim 2, wherein the condition execution instruction is an N-bit instruction.

9. The processor as claimed in claim 1, wherein M is 32 and N is 16.

10. A method capable of executing conditional instructions in a processor, the processor executing an instruction set with M-bit instructions and N-bit instructions (where M, N are positive integers, M>N), the

instruction set having condition execution instructions and M-bit parallel condition execution instructions, the parallel condition execution instruction having a first and a second N-bit instructions, the method comprising:

(A) fetching at least one instruction to be decoded and executed;

(B) when a condition execution instruction is performed, setting a flag to a first logic state if the execution results in a condition acceptance, and setting the flag to a second logic state if the execution results in a condition rejection; and

(C) when the instruction fetched is a parallel condition execution instruction, decoding and executing the first N-bit instruction if the flag is on the first logic state, and decoding and executing the second N-bit instruction if the flag is on the second logic state.

11. The method as claimed in claim 10, wherein the first logic state is "true" and the second logic state is "false".

12. The method as claimed in claim 10, wherein the first logic state is "false" and the second logic state is "true".

13. The method as claimed in claim 10, wherein the condition execution instruction is an M-bit instruction.

14. The method as claimed in claim 10, wherein the condition execution instruction is an N-bit instruction.

15. The method as claimed in claim 10, wherein M is 32 and N is 16.